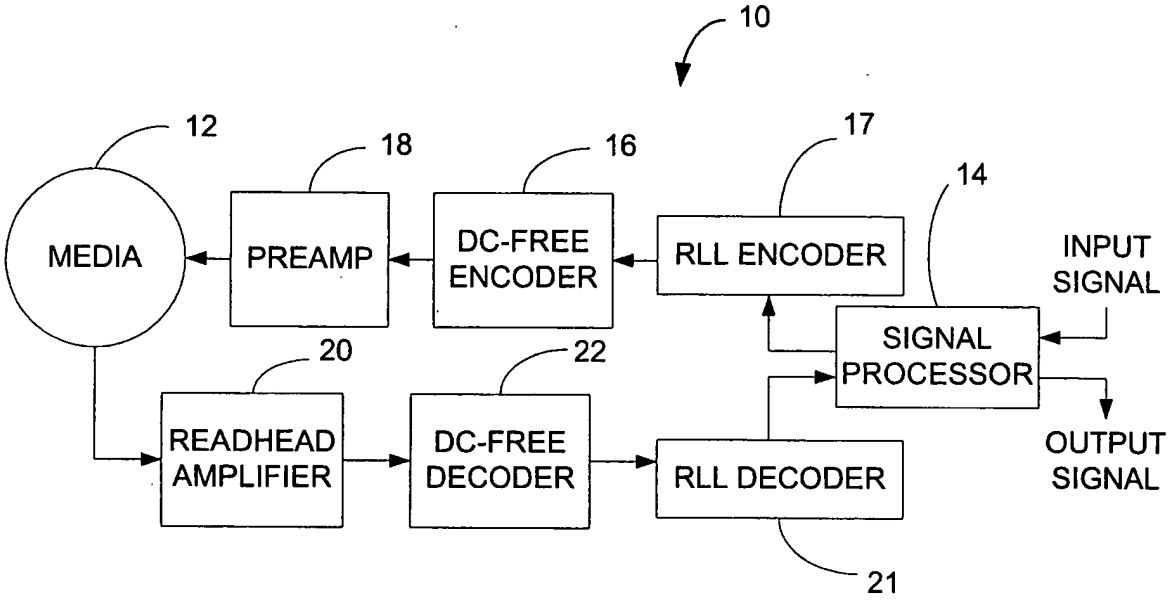
10
12
18
16
17
14
MEDIA
PREAMP
DC-FREE ENCODER
RLL ENCODER
INPUT SIGNAL
SIGNAL PROCESSOR
20
22
READHEAD AMPLIFIER
DC-FREE DECODER
RLL DECODER
OUTPUT SIGNAL
21

FIG. 1

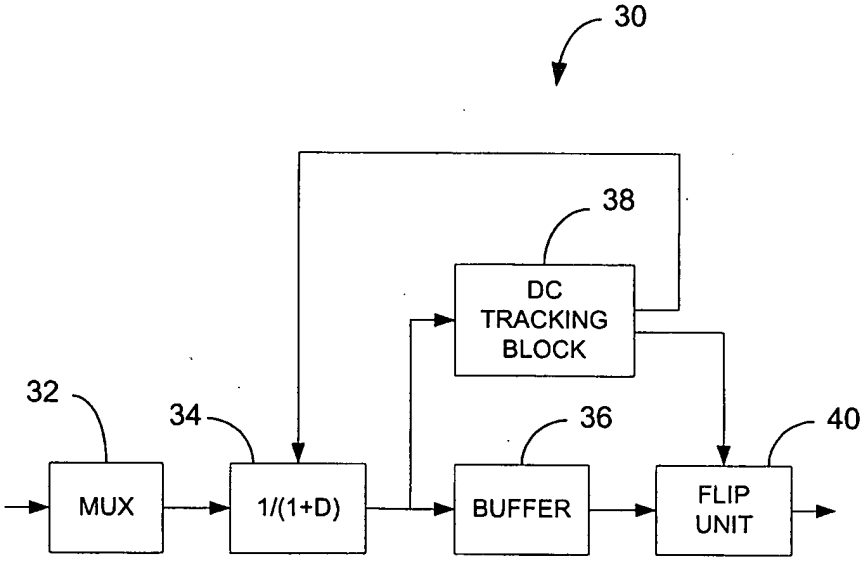
30
38
DC TRACKING BLOCK
32
34
36
40
MUX
1/(1+D)
BUFFER
FLIP UNIT

FIG. 2

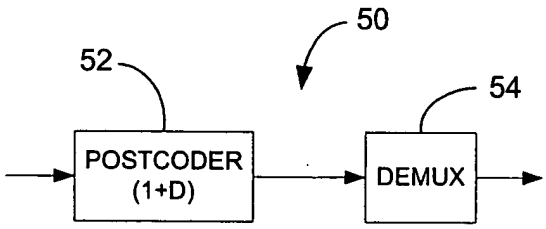

FIG. 3

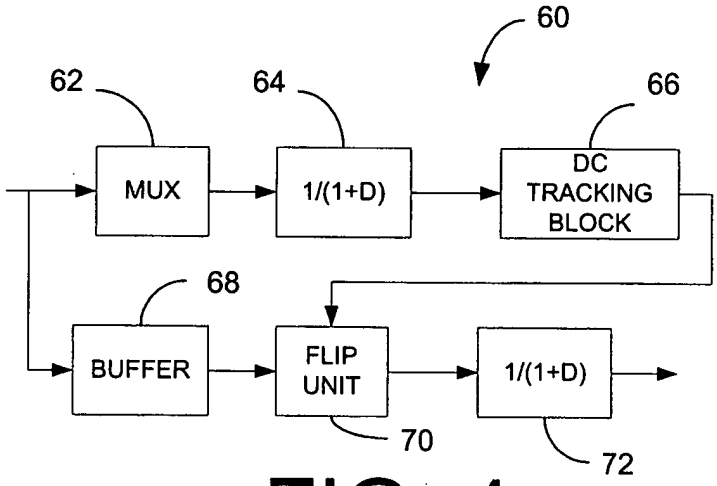

FIG. 4

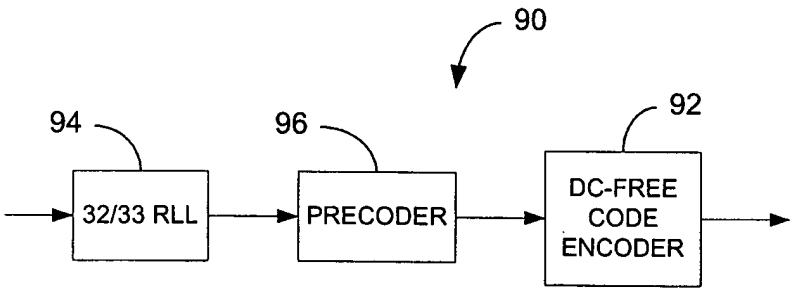

FIG. 6

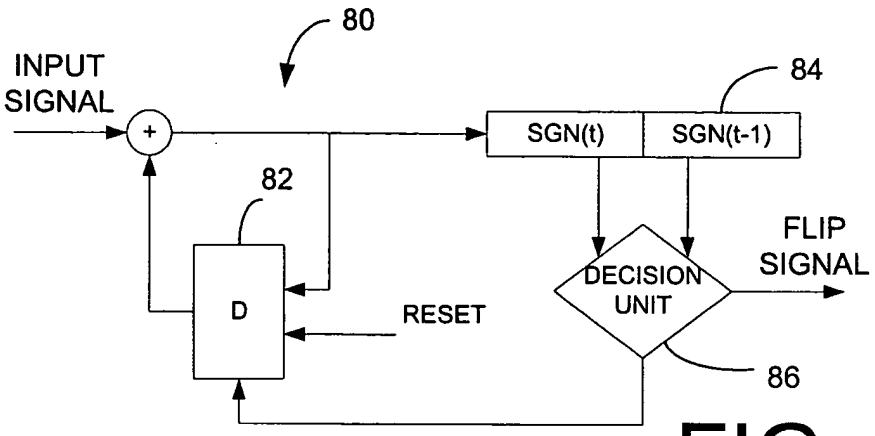

FIG. 5

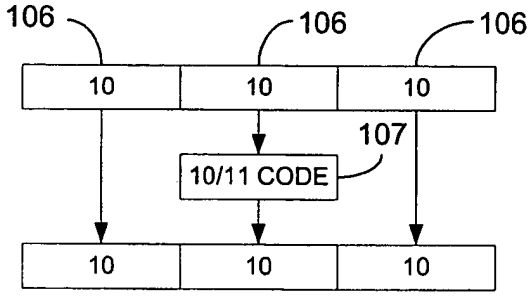

FIG. 7

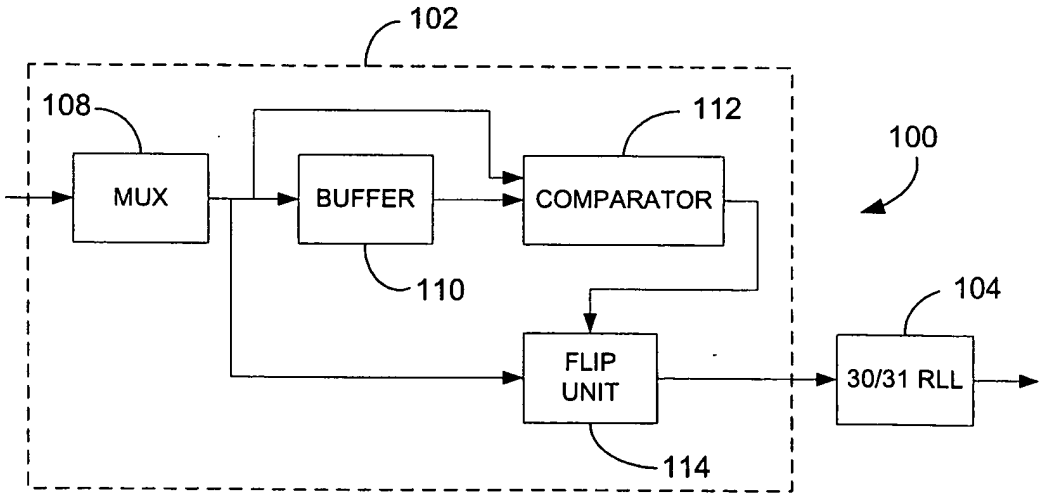

FIG. 8

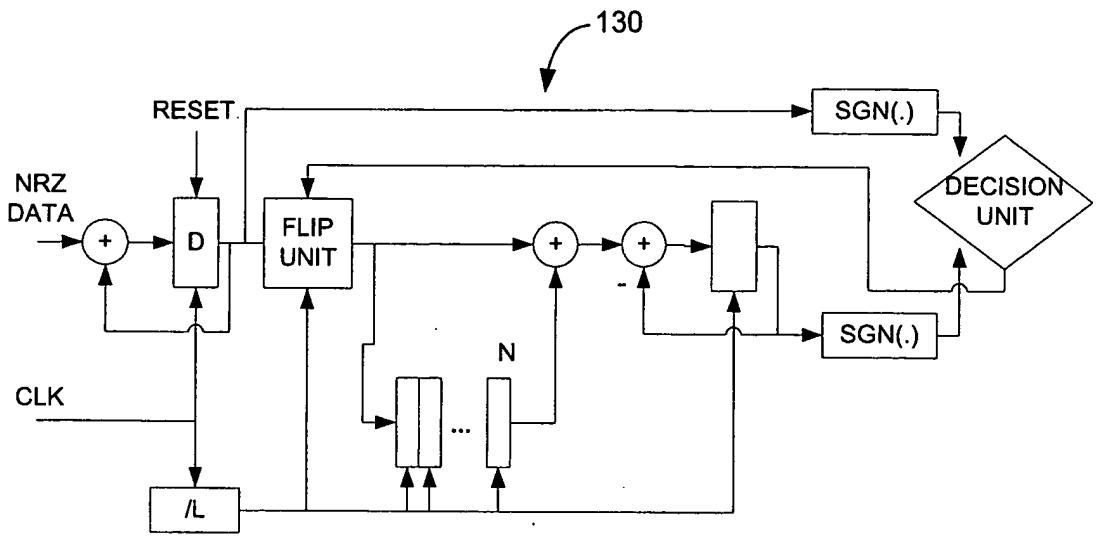
130
RESET
SGN(.)
NRZ
DATA
D
FLIP
UNIT
DECISION
UNIT
N
SGN(.)
CLK
/L

FIG. 9

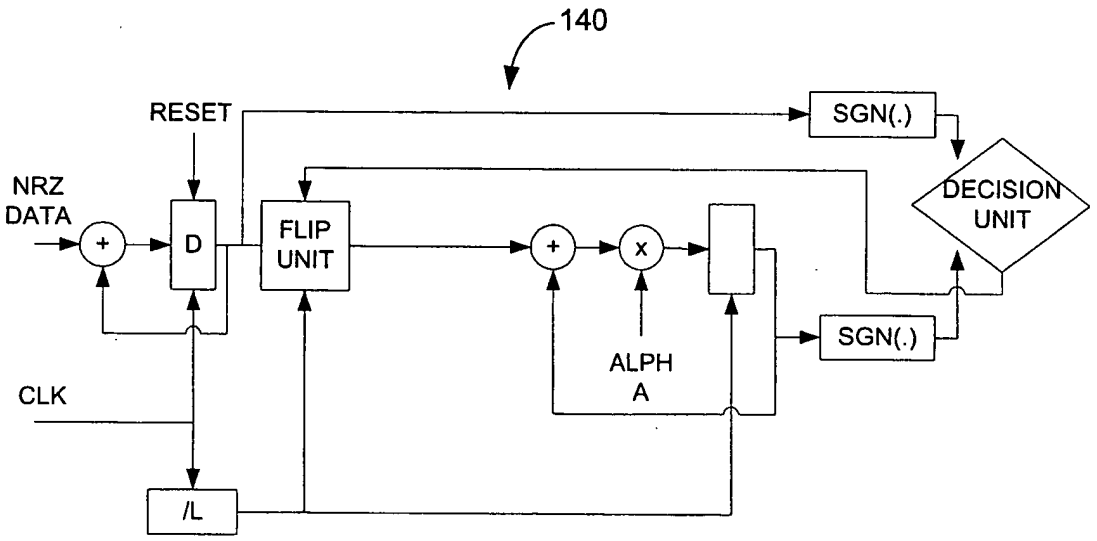
140
RESET
SGN(.)
NRZ
DATA
D
FLIP
UNIT
DECISION
UNIT
x
SGN(.)
ALPH
A
CLK
/L

FIG. 10

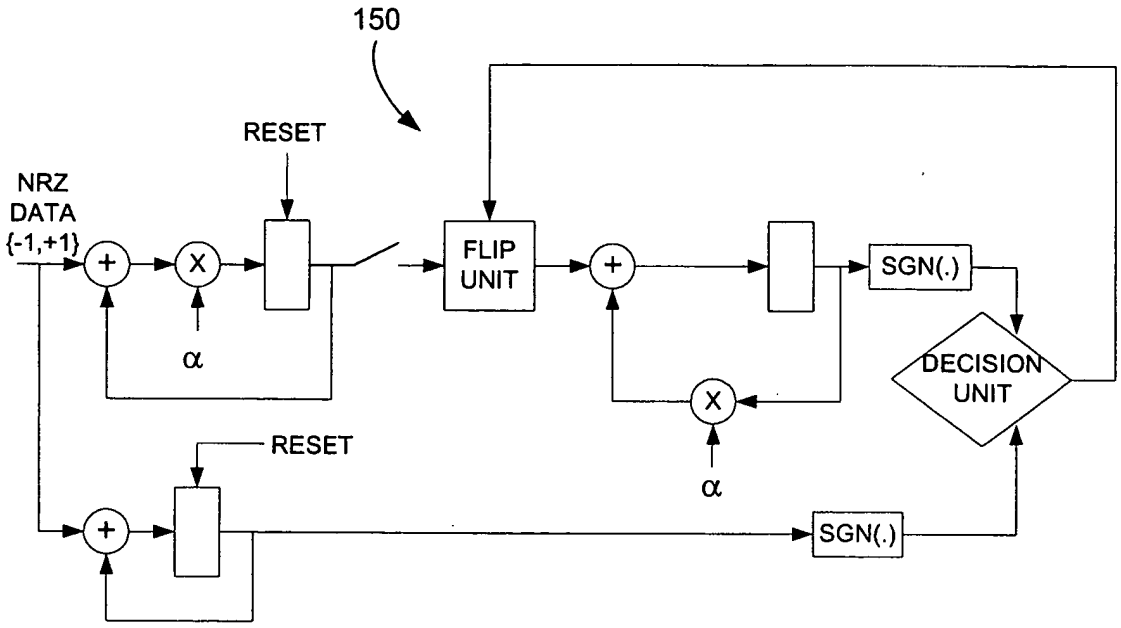
150
RESET
NRZ
DATA
{-1,+1}
+
X
α
FLIP
UNIT
+
SGN(.)
DECISION
UNIT
X
α
RESET
+
SGN(.)

FIG. 11

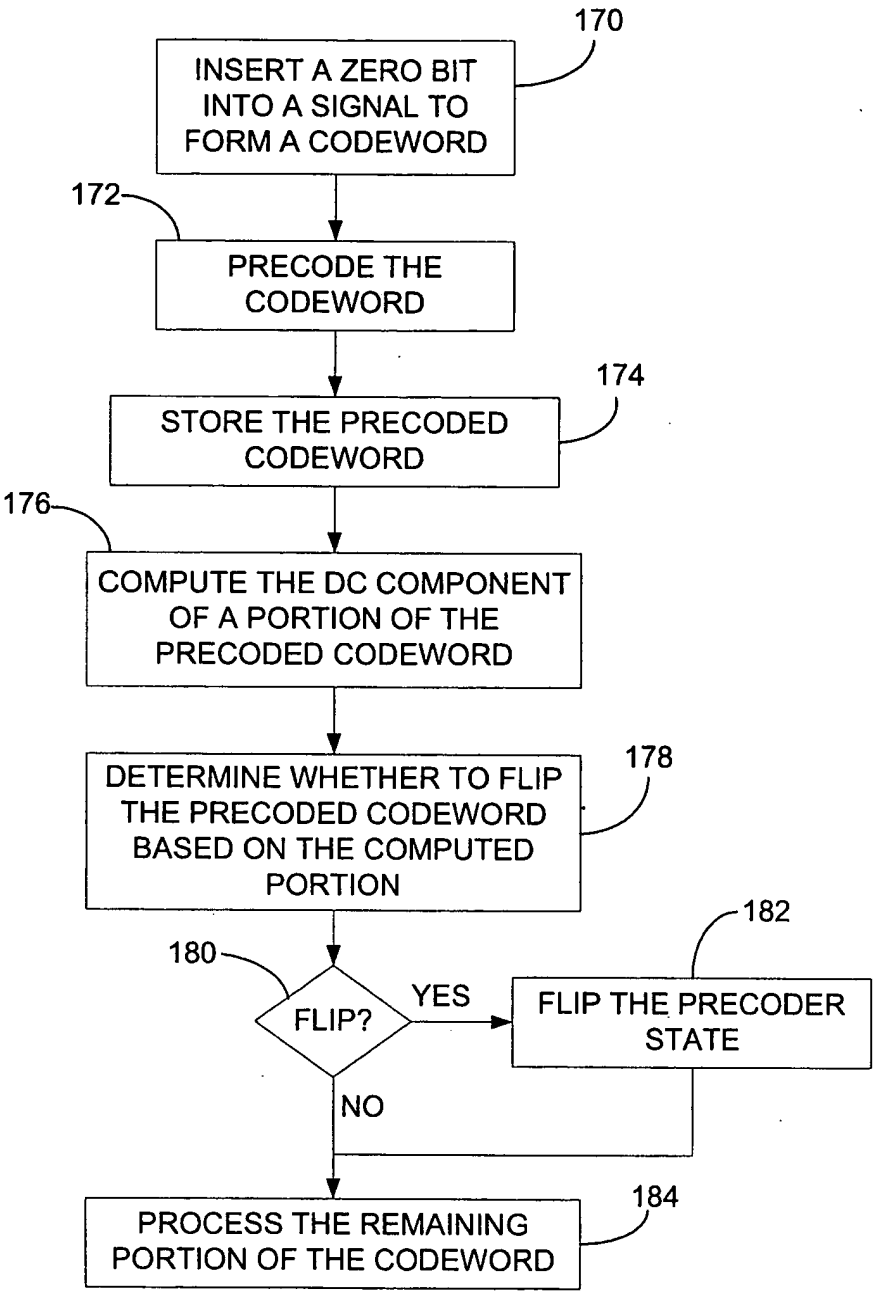
170
INSERT A ZERO BIT INTO A SIGNAL TO FORM A CODEWORD
172
PRECODE THE CODEWORD
174
STORE THE PRECODED CODEWORD
176
COMPUTE THE DC COMPONENT OF A PORTION OF THE PRECODED CODEWORD
178
DETERMINE WHETHER TO FLIP THE PRECODED CODEWORD BASED ON THE COMPUTED PORTION
180
FLIP?
YES
182
FLIP THE PRECODER STATE
NO
184
PROCESS THE REMAINING PORTION OF THE CODEWORD

FIG. 12

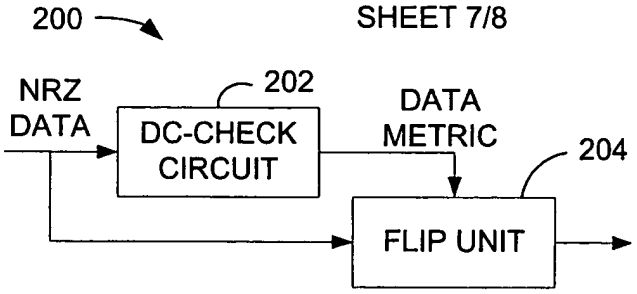

FIG. 13

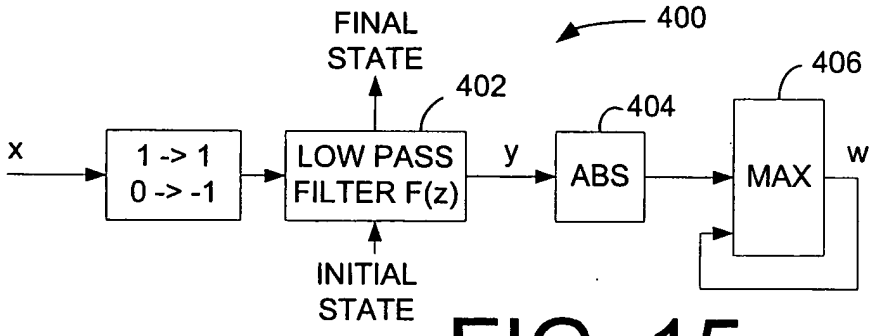

FIG. 15

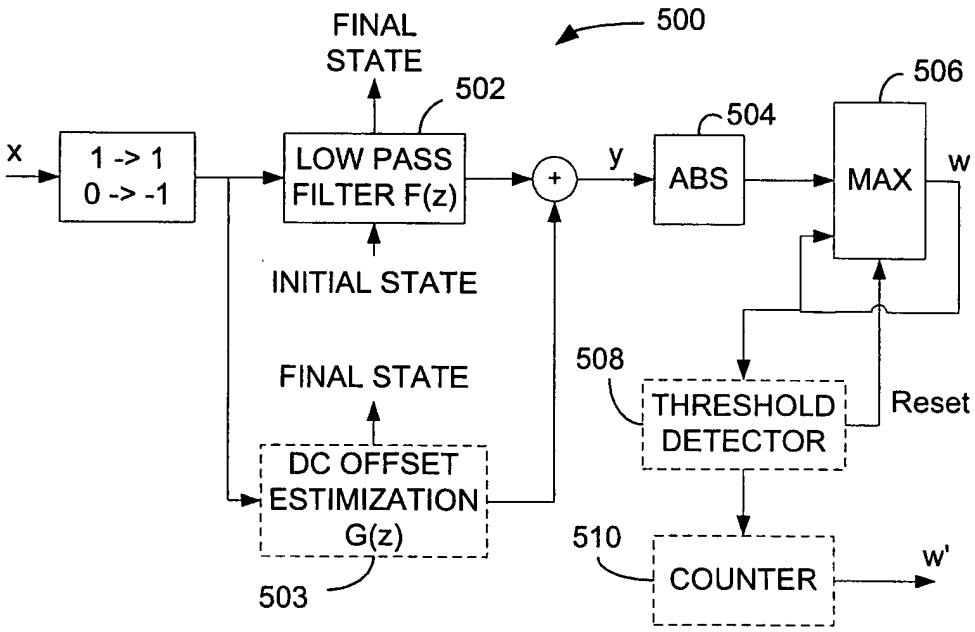

FIG. 16

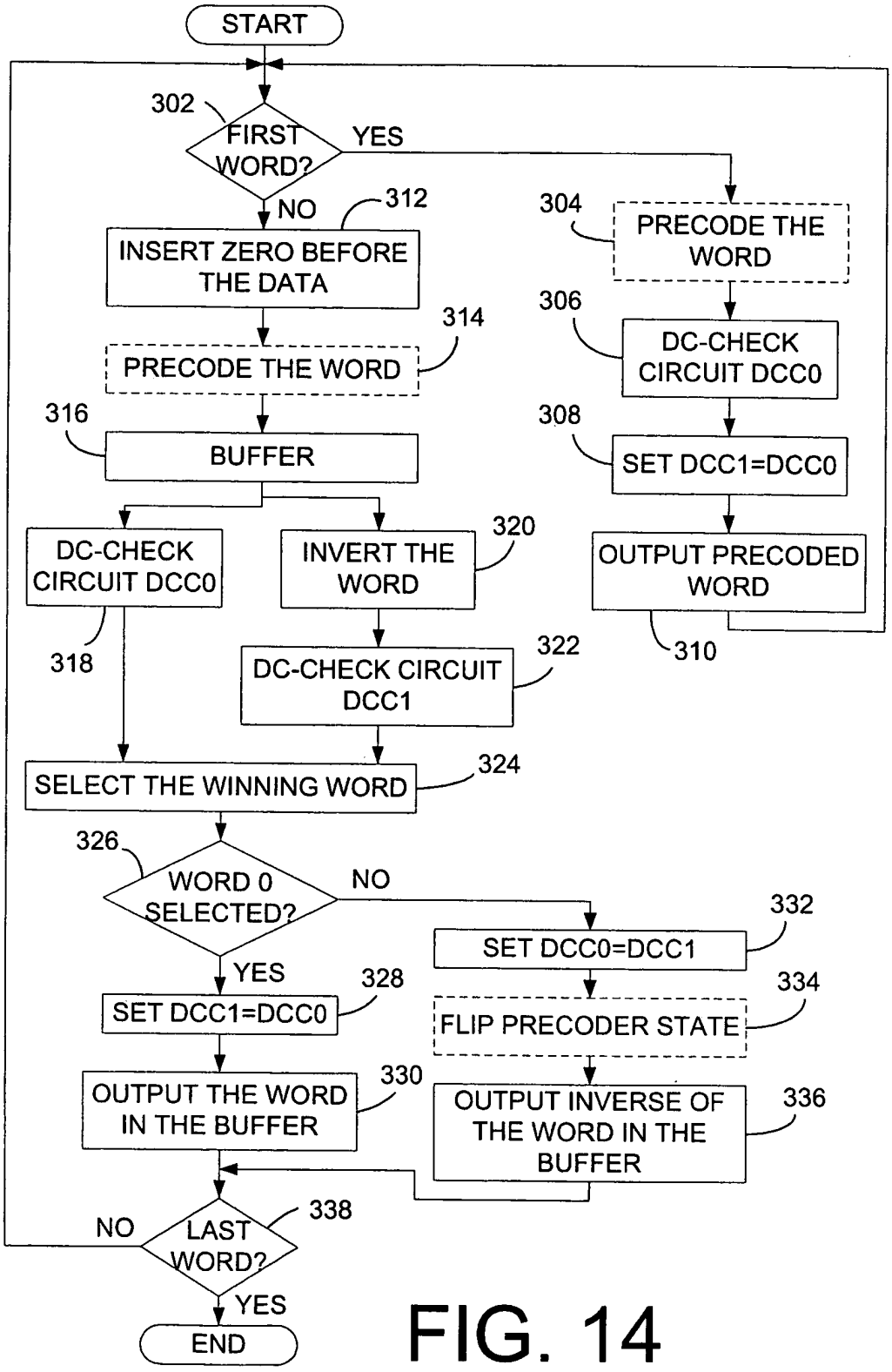
START
302
FIRST WORD?
YES
NO
312
INSERT ZERO BEFORE THE DATA
314
PRECODE THE WORD
316
BUFFER
DC-CHECK CIRCUIT DCC0
318
INVERT THE WORD
320
DC-CHECK CIRCUIT DCC1
322
SELECT THE WINNING WORD
324
326
WORD 0 SELECTED?
NO
YES
328
SET DCC1=DCC0
OUTPUT THE WORD IN THE BUFFER
330
304
PRECODE THE WORD
306
DC-CHECK CIRCUIT DCC0
308
SET DCC1=DCC0
OUTPUT PRECODED WORD
310
332
SET DCC0=DCC1
334
FLIP PRECODER STATE
OUTPUT INVERSE OF THE WORD IN THE BUFFER
336
338
NO
LAST WORD?
YES
END

FIG. 14